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EXAMINER	
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SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/21/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/661,654	LIBERTY ET AL.
	Examiner	Art Unit
	Joseph Schell	2114

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 22-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-9,13-19,22-26,28-30 and 32-37* is/are rejected.

7)☒ Claim(s) *6,10-12,27 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claims 1-19 and 22-37 have been examined.

Claims 6, 10-12, 27 and 31 have been objected to as containing allowable subject matter, yet dependant upon rejected base claims.

Claims 1-5, 7-9, 13-19, 22-26, 28-30, and 32-37 have been rejected.

Response to Arguments

1. Applicant's arguments filed October 10, 2006 have been fully considered but they are not persuasive.

Applicant argues that Beardsley ('631) does not anticipate claims 15 and 22 because Beardsley ('631) does not disclose a plurality of chips in an electric device. The examiner respectfully disagrees. The broadest reasonable interpretation of something being a part of "an electronic device" is being understood by the examiner to mean that the components are part of a physically tangible system that includes electronic components. The data processing system disclosed by Beardsley ('631) does qualify as an electronic device. In Applicant's argument regarding Shima ('476) and Claim 1, Applicant states:

> "The Examiner points to the nodes of Shima, however, Shima states: "Each node is a device (e.g., computer system, digital camera, digital VCR, TV settop box, digital camcorder, storage device, digital audio device... (Shima, col. 7, lines 47-50)." Neither Beardsley nor Shima teach generating timestamps <u>in an electronic device.</u>"

Applicant appears to be implying that because the nodes of Shima ('476) are themselves devices, that the nodes cannot collectively comprise a device. The examiner respectfully disagrees with this logic. As defined by The American Heritage Dictionary (see attached printout), a device is "a contrivance or an invention serving a particular purpose." Devices have no proximity requirements or component integration requirements, and devices can certainly be a part of another device. For example a digital camera (cited by the Shima ('476) excerpt) will generally contain a memory device, a photo-sensor device, and a processing device. And the processing device will generally further contain a memory access device, an execution device, etc. Beardsley ('631) discloses the system for use with a host and peripheral subsystem. The use of "in a device" does not imply limitations not disclosed by Beardsley ('631).

Applicant further argues that Beardsley ('631) does not disclose, as stated in claim 15, "determining an offset between the Time Base and time indicated with each of said local time counters." Examiner respectfully disagrees. Beardsley ('631) column 2 lines 56-61 states that the peripheral subsystem detects events and stores an indication of the event in a log or file along with a time stamp created by the peripheral subsystem clock. Column 2 line 66 through column 3 line 5 describe including a time-correlating log entry that correlates the peripheral subsystem time to the host time.

Finally, the limitation of "each said chip associated with a local time counter" has been emphasized by the Applicant. This limitation is disclosed by Beardsley ('631). Beardsley ('631) discloses one or more host processors associated with at least one subsystem, wherein the subsystem includes a cluster 0 and a cluster 1 (see Figure 1).

Each cluster has a local clock (SCACLK element 31 of Figure 1, and see column 4 lines 15-18 wherein it is explained that the clusters are identical).

Claim Objections

2. Claim 3 line 1 should read "The method of claim 2 wherein said processor..."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 15-17, 22-26, and 28-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Beardsley (US Patent 5,471,631).

4. As per claim 15, Beardsley ('631) discloses an electronic device including at least one processor and a plurality of chips, each said chip associated with a local time counter of a plurality of local time counters, said electronic device including a Time Base selected by said processor, said Time Base being a baseline time value, a method for determining a global ordering of events, said method comprising:

determining an offset between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips (column 3 lines 3-5);

recording each offset associated with each said local time counter at a location accessible to said processor (column 9 lines 53-55, the time-correlation is saved in the SFLOG and column 4 lines 52-60, the host processor can later access the logs for performing problem determinations);

receiving notice at said processor of an event detected with one of said plurality of chips, said notice accompanied by a timestamp generated by said local time counter at the time of the occurrence of said detected event (column 2 lines 54-61, when the host system reads the log it receives the notice of event); and

normalizing said timestamp using said offset, said normalized timestamp being compared with other reported events and associated normalized timestamps to determine an order of occurrence of said events (column 2 lines 58-61, events are saved with peripheral timestamps. Column 2 lines 66-67, time correlation data is also stored).

5. As per claim 16, Beardsley ('631) discloses the method of claim 15 wherein more than one reported timestamp is normalized using said offsets prior to determining said order of occurrence (Beardsley ('631) column 2 lines 58-61, events are saved with peripheral timestamps. Column 2 lines 66-67, time correlation data is also stored. Column 1 lines 46-53, the goal of the system is to facilitation error log reading of a networked system. Because the correlated timestamp is generated to determine an order of events in an error log, it would need to be generated before the determination is made).

6. As per claim 17, Beardsley ('631) discloses the method of claim 15, the further comprising:

determining an offset for an additional time counter associated with an additional chip in said electronic device following the initial determination and recording of said offsets for said plurality of local time counters associated with said plurality of chips (column 7 lines 62-65, a cluster synchronizes its SFCLK with that of a neighbor cluster after initialization, column 8 lines 40-43, the subsystem waits for the "set subsystem time" command from the host and column 6 lines 50-53, an entry in SFLOG is used for correlating times); and

recording said offset at said location accessible to said processor (column 9 lines 53-55, the time-correlation is saved in the SFLOG and column 4 lines 52-60, the host processor can later access the logs for performing problem determinations).

7. As per claim 22, Beardsley ('631) discloses in an electronic device including at least one processor and a plurality of chips, each said chip associated with a local time counter of a plurality of local time counters (column 2 lines 53-54, the current clock time), a medium comprising computer-executable instructions for a method comprising:

detecting an event associated with one of said plurality of chips (column 2 lines 62-66);

generating a timestamp with said local time counter at the time of the occurrence of said detected event, said timestamp being associated with said event (column 2 lines 53-56); and

comparing said event and a normalized form of said timestamp with other events and associated normalized timestamps to determine an order of occurrence (column 3 lines 1-5, events are given a normalized timestamp. Column 5 lines 44-49, the purpose of the timestamp normalization is to allow for correlating event times, meaning that order of occurrence is also determined by the correlating).

8. As per claim 23, Beardsley ('631) discloses the medium of claim 22 wherein said method further comprises:

providing a Time Base selected by said processor, said Time Base being a baseline time value (column 2 lines 47-49, the host time); and

transmitting a reset instruction from said processor to said plurality of local time counters associated with said plurality of chips, said plurality of local time counters resetting to a designated time so as to be synchronized with respect to each other (column 5 lines 51-57, the host processor sends a "set system time" command to selected peripheral subsystems).

9. As per claim 24, Beardsley ('631) discloses the medium of claim 23 where said processor maintains a record of the offset between the reset value of the local time

counter and the Time Base (column 9 lines 44-49, peripheral timestamp and correlated timestamps are both saved in the log).

10. As per claim 25, Beardsley ('631) discloses the medium of claim 23 wherein said designated time is the Time Base and said plurality of local time counters are reset so as to indicate the same time as said Time Base (column 5 lines 51-57, the host processor sends a "set system time" command to selected peripherals, synchronizing them to the host time).

11. As per claim 26, Beardsley ('631) discloses the medium of claim 23 wherein the transmitting of said reset instruction is performed using a simultaneous multicast write operation performed by said processor (column 8 lines 57-63, system time is sent to select clusters of peripheral subsystems).

12. As per claim 28, Beardsley ('631) discloses the medium of claim 23, wherein said method further comprises: resetting all of said plurality of chips and an additional chip, said resetting being performed to add an additional chip that is synchronized with said plurality of chips (column 7 line 49, IML is an initialization procedure, and column 7 lines 62-65, after the IML a cluster synchronizes its clock to another cluster).

13. As per claim 29, Beardsley ('631) discloses the medium of claim 22, wherein said method further comprises:

providing a Time Base in a location accessible to said processor, said Time Base being a baseline time value (column 2 lines 47-49, the host time);

determining an offset between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips (Beardsley ('631) column 3 lines 3-5);

recording each offset associated with each said local time counter at a location accessible to said processor (column 9 lines 53-55, the time-correlation is saved in the SFLOG and column 4 lines 52-60, the host processor can later access the logs for performing problem determinations); and

normalizing the timestamps associated with said detected events using offsets associated with the local time counter generating the timestamps prior to determining said order of occurrence (column 2 lines 58-61, events are saved with peripheral timestamps. Column 2 lines 66-67, time correlation data is also stored. Column 1 lines 46-53, the goal of the system is to facilitation error log reading of a networked system. Because the correlated timestamp is generated to determine an order of events in an error log, it would need to be generated before the determination is made).

14. As per claim 30, Beardsley ('631) discloses the medium of claim 29, wherein said method further comprises:

determining an offset for an additional time counter associated with an additional chip in said electronic device following the initial determination and recording of said offsets for said plurality of local time counters associated with said plurality of chips

(column 7 lines 62-65, a cluster synchronizes its SFCLK with that of a neighbor cluster after initialization, column 8 lines 40-43, the subsystem waits for the "set subsystem time" command from the host and column 6 lines 50-53, an entry in SFLOG is used for correlating times); and

recording said offset at said location accessible to said processor (column 9 lines 53-55, the time-correlation is saved in the SFLOG and column 4 lines 52-60, the host processor can later access the logs for performing problem determinations).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1-5 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beardsley ('631) in view of Shima (US Patent 6,718,476).

16. As per claim 1, Beardsley ('631) discloses in an electronic device including at least one processor and a plurality of chips, each said chip associated with a local time counter of a plurality of local time counters (column 2 lines 53-54, the current clock time) a method for determining a global ordering of events (column 1 lines 49-52), said method comprising:

detecting an event associated with one of said plurality of chips (column 2 lines 62-66);

generating a timestamp with said local time counter at the time of the occurrence of said detected event, said timestamp being associated with said event (column 2 lines 53-56); and

comparing said event and a normalized form of said timestamp with other events and associated normalized timestamps to determine an order of occurrence (column 3 lines 1-5, events are given a normalized timestamp. Column 5 lines 44-49, the purpose of the timestamp normalization is to allow for correlating event times, meaning that order of occurrence is also determined by the correlating).

Beardsley ('631) does not expressly disclose the system wherein the electronic device is an isochronous electronic device.

Shima ('476) teaches a system wherein a group of nodes with local clock synchronization (column 4 lines 29-37 and lines 53-57). The system uses a Firewire compliant bus for communication (column 4 lines 58-60, Standard 1394b).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the timestamp correlating system disclosed by Beardsley ('631) such that it uses an isochronous protocol for data transmission between the nodes. This

modification would have been obvious because isochronous transmission allows for guaranteed bandwidth use with low overhead (Shima ('476) column 1 lines 26-31).

17. As per claim 2, Beardsley ('631) in view of Shima ('476) discloses the method of claim 1, further comprising: providing a Time Base selected by said processor, said Time Base being a baseline time value (Beardsley ('631) column 2 lines 47-49, the host time); and

transmitting a reset instruction from said processor to said plurality of local time counters associated with said plurality of chips, said plurality of local time counters resetting to a designated time so as to be synchronized with respect to each other (Beardsley ('631) column 5 lines 51-57, the host processor sends a "set system time" command to selected peripheral subsystems).

18. As per claim 3, Beardsley ('631) in view of Shima ('476) discloses the method of claim 2 where said processor maintains a record of an offset between the reset local time counter time and the Time Base (Beardsley ('631) column 9 lines 44-49, peripheral timestamp and correlated timestamps are both saved in the log).

19. As per claim 4, Beardsley ('631) in view of Shima ('476) discloses the method of claim 2 wherein said designated time is the Time Base and said plurality of local time counters are reset so as to indicate the same time as said Time Base (Beardsley ('631)

column 5 lines 51-57, the host processor sends a "set system time" command to selected peripherals, synchronizing them to the host time).

20. As per claim 5, Beardsley ('631) in view of Shima ('476) discloses the method of claim 2 wherein said transmitting of said reset instruction is performed using a simultaneous multicast write operation performed by said processor (Beardsley ('631) column 8 lines 57-63, system time is sent to select clusters of peripheral subsystems).

21. As per claim 7, Beardsley ('631) in view of Shima ('476) discloses the method of claim 2, further comprising: resetting all of said plurality of chips and an additional chip, said resetting being performed to add the additional chip that is synchronized with said plurality of chips (Beardsley ('631) column 7 line 49, IML is an initialization procedure, and column 7 lines 62-65, after the IML a cluster synchronizes its clock to another cluster).

22. As per claim 8, Beardsley ('631) in view of Shima ('476) discloses the method of claim 1, further comprising:

providing a Time Base selected by said processor, said Time Base being a baseline time value (Beardsley ('631) column 2 lines 47-49, the host time);

determining an offset between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips (Beardsley ('631) column 3 lines 3-5);

recording each offset associated with each said local time counter at a location accessible to said processor (Beardsley ('631) column 9 lines 53-55, the time-correlation is saved in the SFLOG and column 4 lines 52-60, the host processor can later access the logs for performing problem determinations); and

normalizing the timestamps associated with said detected events using offsets associated with the local time counter generating the timestamps prior to determining said order of occurrence (Beardsley ('631) column 2 lines 58-61, events are saved with peripheral timestamps. Column 2 lines 66-67, time correlation data is also stored. Column 1 lines 46-53, the goal of the system is to facilitation error log reading of a networked system. Because the correlated timestamp is generated to determine an order of events in an error log, it would need to be generated before the determination is made).

23. As per claim 9, Beardsley ('631) in view of Shima ('476) discloses the method of claim 8, further comprising:

determining an offset for an additional time counter associated with an additional chip in said electronic device following the initial determination and recording of said offsets for said plurality of local time counters associated with said plurality of chips (Beardsley ('631) column 7 lines 62-65, a cluster synchronizes its SFCLK with that of a neighbor cluster after initialization, column 8 lines 40-43, the subsystem waits for the "set subsystem time" command from the host and column 6 lines 50-53, an entry in SFLOG is used for correlating times); and

recording said offset at said location accessible to said processor (Beardsley ('631) column 9 lines 53-55, the time-correlation is saved in the SFLOG and column 4 lines 52-60, the host processor can later access the logs for performing problem determinations).

24. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beardsley ('631) in view of Shima ('476) as applied to claim 1, and in further view of Meltzer (US Patent 4,852,095).

Beardsley ('631) in view of Shima ('476) discloses the method of claim 1. Beardsley ('631) in view of Shima ('476) does not expressly disclose the method wherein each said chip is associated with a local event register, said local event register recording the occurrence of a hardware event associated with said chip.

Meltzer ('095) teaches an error detection system for multiple FRUs (see abstract and Figure 1). The system includes a counter that indicates which FRU first reported an error (column 2 lines 8-100).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Beardsley ('631) such that each peripheral has an associated counter for error indication. This modification would have been obvious because some errors propagate between subsystems quickly making it difficult to

determine where the error originated (Meltzer ('095) column 1 lines 18-22) and the error reporting register identifies which unit first experienced the error (Meltzer ('095) column 2 lines 2-8).

25. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beardsley ('631) in view of Shima ('476) as applied to claim 1, and in further view of Fisher (US Patent 6,334,191).

Beardsley ('631) in view of Shima ('476) discloses the method of claim 1. Beardsley ('631) in view of Shima ('476) does not expressly disclose the medium wherein more than one of said plurality of chips is associated with the same local time counter.

Fisher ('191) teaches a system wherein a single timer generates output events for multiple I/O devices (column 1 lines 39-42).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Beardsley ('631) such that multiple clusters share the same timer circuitry as disclosed by Fisher ('191). This modification would have been obvious because it allows for decreased hardware costs and design flexibility (Fisher ('191) column 1 lines 32-35).

26. Claims 18, 32, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beardsley ('631) in view of Pawlowski ('551).

27. As per claim 18, Beardsley ('631) discloses the method of claim 16 wherein a timestamp received from the host is associated with said reported event and timestamp and used in determining said order of occurrence of events (column 5 lines 44-48, the timestamp received from the host is used for determining offset. And column 3 lines 1-5, the offset is used for putting all event times into host time, which allows for an accurate order of occurrence to be determined).

Beardsley ('631) does not expressly disclose the method wherein the timestamp is from software or from the operating system.

Pawlowski ('551) teaches a system that checks the status of I/O (see abstract). The system also makes use of software timers initiated from a time of day clock (column 12 lines 27-31).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Beardsley ('631) in view of Shima ('476) such that the host time is a software timer associated with the host system's operating system. This modification would have been obvious because a "time of day" clock is running on most

computers and it's use requires no additional hardware (Pawlowski ('551) column 12 lines 30-36).

28. As per claim 32, Beardsley ('631) discloses the medium of claim 22 wherein a timestamp received from the host is associated with said reported event and timestamp (column 5 lines 51-54).

Beardsley ('631) does not expressly disclose the method wherein the timestamp is from software or from the operating system.

Pawlowski ('551) teaches a system that checks the status of I/O (see abstract). The system also makes use of software timers initiated from a time of day clock (column 12 lines 27-31).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Beardsley ('631) in view of Shima ('476) such that the host time is a software timer associated with the host system's operating system. This modification would have been obvious because a "time of day" clock is running on most computers and it's use requires no additional hardware (Pawlowski ('551) column 12 lines 30-36).

29. As per claim 33, Beardsley ('631) in view of Pawlowski ('551) discloses the medium of claim 32 wherein said software timestamp is used in determining said order of occurrence of events (Beardsley ('631) column 5 lines 44-48, the timestamp received from the host is used for determining offset. And column 3 lines 1-5, the offset is used for putting all event times into host time, which allows for an accurate order of occurrence to be determined).

30. Claims 19 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beardsley ('631) in view of Meltzer ('095).

31. As per claim 19, Beardsley ('631) discloses the method of claim 16. Beardsley ('631) does not expressly disclose the method wherein each said chip is associated with a local event register, said local event register recording the occurrence of a hardware event associated with said chip.

Meltzer ('095) teaches an error detection system for multiple FRUs (see abstract and Figure 1). The system includes a counter that indicates which FRU first reported an error (column 2 lines 8-100).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Beardsley ('631) such that each peripheral has an associated counter for error indication. This modification would have been obvious

because some errors propagate between subsystems quickly making it difficult to determine where the error originated (Meltzer ('095) column 1 lines 18-22) and the error reporting register identifies which unit first experienced the error (Meltzer ('095) column 2 lines 2-8).

32. As per claim 34, Beardsley ('631) discloses the medium of claim 22. Beardsley ('631) does not expressly disclose the medium wherein an indication of said detected event is stored in a local event register.

Meltzer ('095) teaches an error detection system for multiple FRUs (see abstract and Figure 1). The system includes a counter that indicates which FRU first reported an error (column 2 lines 8-100).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Beardsley ('631) such that each peripheral has an associated counter for error indication. This modification would have been obvious because some errors propagate between subsystems quickly making it difficult to determine where the error originated (Meltzer ('095) column 1 lines 18-22) and the error reporting register identifies which unit first experienced the error (Meltzer ('095) column 2 lines 2-8).

33. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beardsley ('631) in view Fisher (US Patent 6,334,191).

Beardsley ('631) discloses the medium of claim 22. Beardsley ('631) does not expressly disclose the medium wherein more than one of said plurality of chips is associated with the same local time counter.

Fisher ('191) teaches a system wherein a single timer generates output events for multiple I/O devices (column 1 lines 39-42).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the system disclosed by Beardsley ('631) such that multiple clusters share the same timer circuitry as disclosed by Fisher ('191). This modification would have been obvious because it allows for decreased hardware costs and design flexibility (Fisher ('191) column 1 lines 32-35).

34. Claims 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Addink (US Patent 6,042,477) in view of Johnson (US Patent 4,742,511).

35. As per claim 36, Addink ('477) discloses a method, comprising:

providing a baseline time value selected by a processor (column 3 lines 1-5, the receiving computer has a base clock, the offset from which is calculated, the processor is the server of column 4 line 66 through column 5 line 7);

generating a packet on a first chip, wherein the first chip is controlled by the processor (column 5 lines 10-11, each client computer sends packets to the server, the server controls the processors, column 4 lines 66-67);

generating a first timestamp upon generating the packet on the first chip, wherein the first timestamp is generated by a first local time counter resident on the first chip (column 2 lines 55-60);

forwarding the first timestamp to the processor (column 5 lines 10-11, the computers send packets to the server);

normalizing the first timestamp with respect to the baseline time value (column 5 lines 43-48);

generating a packet on a second chip, wherein the second chip is controlled by the processor (column 4 lines 18-22 and 36-40, each PC has a player);

generating a second timestamp upon generating the packet on the second chip, wherein the second timestamp is generated by a second local time counter resident on the second chip (column 2 lines 55-60);

forwarding the second timestamp to the processor (column 5 lines 10-11, the computers send packets to the server);

normalizing the second timestamp with respect to the baseline time value (column 5 lines 43-48); and

comparing the normalized first timestamp with the normalized second timestamp to determine if the packet on the first chip occurred before the packet on the second chip (column 6 line 56 through column 7 line 2, and column 7 lines 16 through 20, in determining the position of each target "for all time," the receiving server must also determine when each packet occurred and in what order).

Addink ('477) teaches a timestamp correlating system for use with computer games over a network. Addink ('477) does not expressly disclose the system wherein the providing a packet is in response to detecting an error.

Johnson ('511) teaches a packet routing network using a lookup table at each node to determine the shortest path for routing (see abstract). Johnson ('511) additionally teaches the generation of an error packet upon a link failure and resend failure a set number of times (Figure 9 step 258).

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the timestamp correlating system disclosed by Addlink ('477) such that a fault packet is generated at a node. This modification would have been obvious because the use of an error notification packet on link failure contributes toward a fault tolerant network (Johnson ('511) column 2 lines 35-36).

36. As per claim 37, Addink ('477) in view of Johnson ('511) discloses the method of claim 36, wherein the processor normalizes the first timestamp after the first timestamp is forwarded to the processor (Addink ('477) column 6 lines 50-55, the offset is calculated after receiving a packet).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Schell whose telephone number is (571) 272-8186. The examiner can normally be reached on Monday through Friday 9AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS

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SUPERVISORY PATENT EXAMINER